

Security & Chip Card ICs

SLF9000 Terminal IC

Terminal IC for Contactless Chip Cards according ISO 14443- Type A and B

SLF9000 Short Product Information								
This document contains preliminary information on a new product under development. Details are subject to change without notice.								
Revision History: Current Version 05.00								
Previous Releases: 03/99, 09/99 (former product name: ISO-CLL)								
Page	Subjects (changes since last revision)							
2	Contact phone and fax number changed							
8	Package type description							

Important: Further information is confidential and on request. Please contact:

Infineon Technologies AG in Munich, Germany,

Security & Chip Card ICs, Phone +49-89-234-80000 Fax +49-89-234-81000

E-Mail: security.chipcard.ics@infineon.com

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The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives world-wide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

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Terminal IC for Contactless Chip Cards according ISO 14443- Type A/B with multiplexed/ demultiplexed 8- bit parallel interface

Features

- Carrier freq. 13.56 MHz
- Data rate 106 Kbit/s
- Data transparent
- Register driven operation
- all ISO 14443 protocols supported
- additional other protocol (e.g. type B2 -fast Siemens)
- Frame length up to 128 bytes
- Type A (e.g. Mifare), deterministic anticollision procedures supported by HW
- 8-bit parallel interface with three selectable modes:
 - non-multiplexed
 - multiplexed (Intel compatible)
 - Enhanced Parallel Port (EPP) interface
- 128 Byte FIFO for burstwise data transmission/ reception
- Transmission error detection by CRC according ISO 3309 and CCITT-16 with programmable CRC modes
- Optional odd parity handling
- Supports inexpensive external single Analog Interface (AIF)
- Free programmable 16 bit hardware timer e.g. for real time operation

Encoders

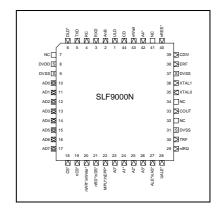
- Transaction speed: 106 Kbit/s according to ISO 14443
- Cascade level operation supported

Decoders

- Slot marker operation possible
- Decoding algorithm parameters adjustable
- Any number of time slots supported

Table 1 Ordering Information

Туре	Package	Option
SLF9000N	PLCC 44	Q67100-Z3104





1 Pin Description

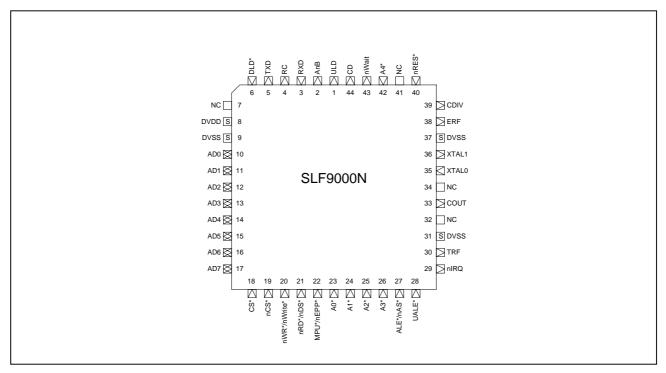


Figure 1 Pin Configuration (top view)

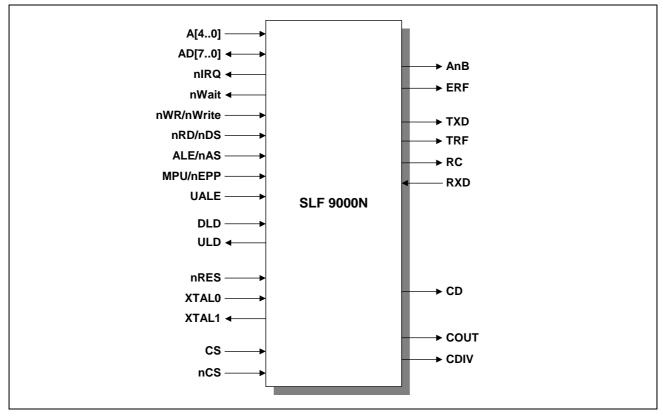


Figure 2 Pad Configuration



Table 2 Pin Definitions and Functions

Pin	Symbol	Function								
8	DVDD	Digital supply voltage (+ 3.3/5V)								
9, 31, 37	DVSS	Digital ground (GND)								
40	nRES	Reset input, low-active								
35	XTAL0	Xtal input: oscillating signal of a simple 13.56 MHz crystal here or external oscillator sqaure wave								
36	XTAL1	Xtal driver: crystal driver output , left open if external oscillator used								
33	COUT	Clock out: 13.56 MHz clock outp	Clock out: 13.56 MHz clock output signal (e.g. for AIF)							
39	CDIV	Clock divisions: 13.56 MHz clock divided by multiples of 2 or 3 for environmental circuits (divider rate adjustable by internal register settings)								
29	nIRQ	Interrupt output, allows interrupt operation (active level adjustable by reg.)								
2	AnB	Type A not B: type selection ou when low	tput to AIF; type A when high, B							
38	ERF	Enable RF: directs AIF to switch	Enable RF: directs AIF to switch on/off RF signal							
5	TXD	Transmit- signal to Analog Interface (AIF)								
30	TRF*	TXD with RF: signal shape of TXD combined with 13.56 MHz								
4	RC*	Residual carrier; type B residual carrier to drive small RF units directly								
3	RXD	Receive- signal from AIF								
44	CD	Collision detected: extra line to monitor a collision in serial operation								
1	ULD	Uplink data: serial digital output of decoded data from the AIF								
6	DLD	Downlink data: serial digital input to the encoder for direct mooperation								
22	MPU/nEPP	MPU mode when high	nable EPP mode when low							
42,26,25,24,23	A[40]	5-bit address bus for non multiplexed mode (see UALE)								
17,16,15,14, 13,12,11,10	AD[70]	Data (and address; see UALE) bus, 8 bit	Multiplexed address / data bus							
28	UALE	use ALE; multiplexed MPU interface when high	-chip test mode-							
27	ALE/nAS	Address latch enable;strobe for the internal address latch when using a multiplexed MPU inter- face (see UALE), high active	Address strobe, low active; latch AD bus into internal address latch							
43	nWait		EPP Port ready when high							
20	nWR/nWrite	Write strobe in MPU mode; Write on selected register selected by addresses when low, Read from high								



Pin	Symbol	Function							
21	nRD/nDS	Read strobe, low active	data strobe, low active; AD pattern is data						
18	CS	Chip select: enables MPU IF when high (functional AND wired to nCS)							
19	nCS	not chip select: enables the MPU IF when low (functional AND wired to CS)							

n..: active low ...*: high load output signals



2 Description

The SLF9000 (<u>ISO</u>14443 compatible <u>C</u>ontact<u>l</u>ess <u>L</u>ogic- IC) is a transparent contactless terminal IC. It features as a link between an analog interface (AIF) for RF based contactless chip cards (PICC) and a given host system.

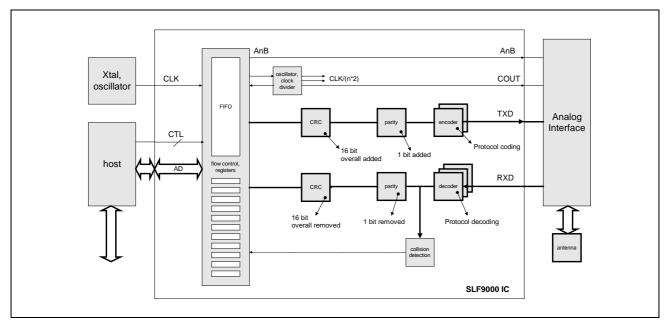


Figure 3 Block Diagram

The SLF9000 is fully register controlled. It performs the encoding and decoding of data according ISO 14443 (Type A and B). Additionally CRC- and parity bits may be added by setting the dedicated control registers. These settings are widely independent and adjustable by software: coding style (Miller/NRZ), error correction (CRC/ Parity), anticollision (Mifare® deterministic/ slotted aloha), decoder type (Manchester/ BPSK).

The SLF9000 offers two kinds of host interfaces. The <u>E</u>nhanced <u>P</u>arallel <u>P</u>ort (EPP) Interface is dedicated for evaluation and debugging purposes or lowest cost solutions. The parallel port of a standard personal computer can be used to directly address and supply the registers of the SLF9000 with data (multiplexed 8bit-data/address bus). The MPU Interface opens a variety of system integrated solutions with serial (e.g. RS232, RS 422) or bus oriented (e.g. RS485, USB, Firewire, IIC, PCI, ISA) interfaces to the host system. It serves mass production and stand alone PCDs (PCD = Proximity Coupling Device).

The SLF9000 supports low cost external single Analog Interface (AIF) for modulation and demodulation of type A and B systems with a carrier frequency of 13.56 MHz. The SLF9000 provides ample information on the current status of the contactless interface. As many cards operate on antennas the information may be used to perform collision detection and to handle transmission errors by software.

The SLF9000 does not perform security functions by hardware. All authentication may be for example a task of the host system. Accordingly, all security information is kept centrally on the host system. Security attacks against the terminals have no effect.



3 Package and Dimensions

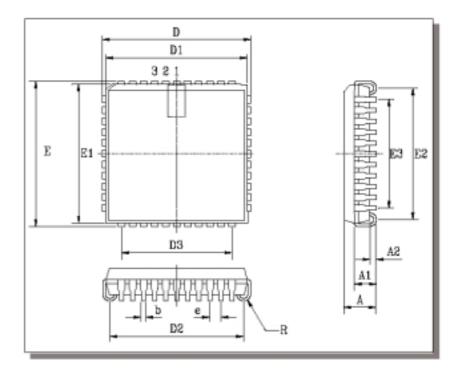


Figure 4 PLCC44

Table 3 Chip Dimensions (inch)

Plastic Leaded Chip Carrier (PLCC)

PLCC 44

Package Type		D/E	D1/E1	D2/E2	D3/E3	Α	A 1	A2	е	b	R
	min	0.685	0.650	0.590		0.165	0.090	0.020		0.013	0.025
PLCC 44					0.500				0.050		
. <u></u>	max	0.695	0.656	0.630		0.180	0.120			0.021	0.045

Dimension: inch, coplanarity < 0.04", original dimension: inch

Table 4 Chip Dimensions (mm)

Plastic Leaded Chip Carrier (PLCC)

PLCC 44

Package Type		D/E	D1/E1	D2/E2	D3/E3	Α	A1	A2	е	b	R
	min	17.40	16.51	14.99		4.20	2.29	0.51		0.33	0.64
PLCC 44					12.70				1.27		
	max	17.65	16.66	16.00		4.57	3.04			0.53	1.14

Dimension: inch, coplanarity < 0.1 mm, original dimension: inch